

A 12.5 GHz-Band 50W Solid-State Power Amplifier for Future Broadcasting Satellites

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ABSTRACT

We designed and fabricated a 50W solid-state power amplifier(SSPA) utilizing a cylindrical cavity type power combiner with low-insertion loss and a corporate type power divider. The isolation between the input ports of the combiner is studied. The output power of the SSPA is more than 50W over a bandwidth of 12.625 ± 0.125 GHz, its efficiency is more than 21.6% including electronic power conditioners(EPCs)(more than 26% excluding the EPCs). The gain is more than 37dB. A thermal vacuum test was put into operation, resulting in satisfactory performance.

INTRODUCTION

In Japan, a round-the-clock broadcasting service using BS-2b was started on July 4, 1987. BS-3a is scheduled to be launched in this summer. It will be equipped with six 120W TV transponders to deliver a three-channel broadcasting service and one 20W broad-band transponder. Although the power amplifier of the latter uses a 20W TWTA, the broad-band transponder on future broadcasting satellites will have an output power of more than several tens of watts and SSPA will be required.

We have, therefore, developed SSPAs mainly by researching low-loss power combiners, which are key components for SSPAs.

This paper presents the design and the performance of an SSPA, especially a power combiner with low loss and of a small size. It also proposes a simple method of calculating the scattering parameters of a combiner, which is used to evaluate the isolation between the input ports of the combiner, through data obtained using eigenvector excitation measurement. The performance of the SSPA under a thermal vacuum test is described. The graceful degradation property is also shown, which is important in the performance of SSPAs.

CONSTRUCTION OF SSPA

The block diagram of the SSPA is shown in Fig.1. To increase the efficiency of SSPAs, the arrangement of the

FETs is as important as decreasing the insertion loss of the combiners. The arrangement of the FETs was designed taking the property of the FETs into account so that the SSPA has maximum efficiency. The SSPA consists of a drive amplifier with two output ports, two 4-way power dividers using an E-plane bend, eight power amplifier units, and an 8-way power combiner with waveguide inputs and output. The drive amplifier has three stages of GaAs FETs, and operates in the linear region. Its output power is 28.7dBm. The configuration of the SSPA is radial, and can easily maintain the same electrical and thermal characteristics for each power amplifier unit. A photograph of the SSPA is shown in Fig.2. The dimensions of the SSPA is 340×390×130 mm.

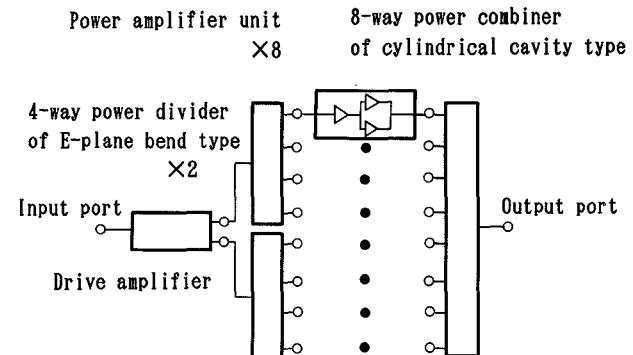


Fig.1 Block diagram of SSPA

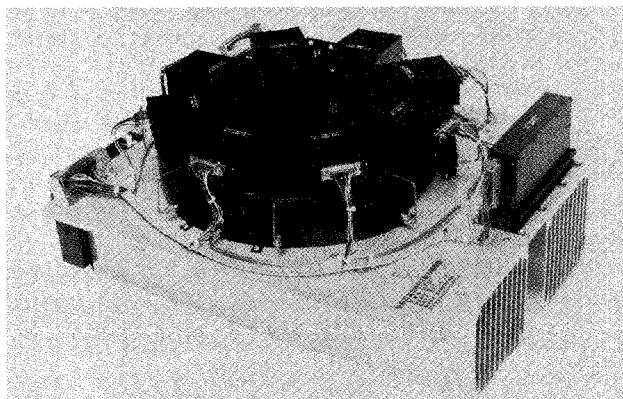


Fig.2 Photograph of SSPA

DESIGN AND EVALUATION OF POWER COMBINER

The structure of the power combiner is shown in Fig.3. To have the properties of low loss and small size, the 8-way power combiner is made of a cylindrical cavity which combines the output power of each power amplifier at the same time. The number of input ports of the combiner was determined as follows. As the output power of each power amplifier unit is 8W, it is necessary for obtaining 50W output power from a SSPA that the number of combined units is more than or equal to 7. When the combiner has more than 8 input ports, we have difficulty in getting isolation between the input ports of the combiner. The input ports are R120 waveguides, and the output port is a TM₀₁ mode circular waveguide. The output power of the combiner is extracted from a rectangular waveguide by means of a TM₀₁-TE₁₀ mode converter. The combiner uses TM₀₄₀ mode. The order of the modes was selected by a trade-off of the following. A combiner with a large cavity is preferable to attach eight input ports to the combiner. Namely, a higher order of mode is needed. On the other hand, a lower order of mode is better for increasing the bandwidth of the combiner(1).

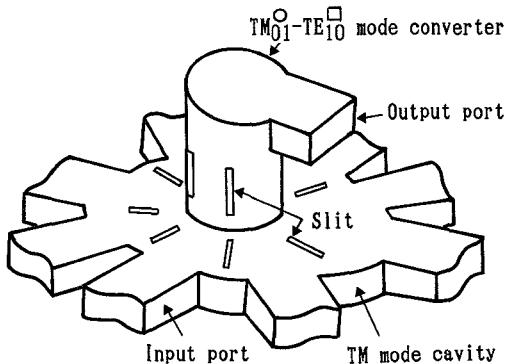


Fig.3 Structure of power combiner

The dimensions of the combiner are as follows(2). ① The Y parameters of the combiner as the two-aperture waveguide circuit including the resonator are given by the variational method. These Y parameters are translated into the Y parameters of an N-way power combiner(2). ②The matching condition is obtained from the image parameters calculated from the Y parameters. From this procedure, the dimensions of the cavity and the iris for adjustment of the coupling between the input waveguides or output waveguide and the cavity can be found.

The insertion loss and return loss at the output port are shown in Fig.4 over the bandwidth of 12.625±0.125GHz. The former is less than 0.3dB and the latter is more than 22dB.

Isolation can be thought of as maintaining a small deviation of the return loss at each input port of the

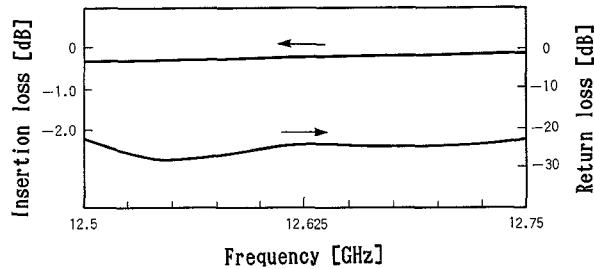


Fig.4 Insertion loss and return loss at output port of combiner

combiner, when some power amplifier units break down. A large isolation can avoid the influence of any failed amplifiers on the other normal power amplifier units. The role of the slits in the combiner as shown in Fig.3 is to achieve a suitably large isolation between the input ports through the absorption of spurious modes that do not contribute to the power combinations. The shapes and positions of the slits are so decided that they minimize the $\max |S_{ij}|$ ($i, j=1, 2, \dots, N$) of the combiner, even if one or more power amplifier units fail.

To obtain the S-parameters of the combiner, we recently introduced a simple method using eigenvector excitation measurement. An N-way combiner matrix generally has $N+1$ rows and columns. The submatrix for the input ports has N rows and columns and is given by $[S]$. Because of the circular symmetry of the combiner, the k-th element, x_{ik} , of the i-th eigenvector of the $N \times N$ submatrix $[S]$ is given by

$$x_{ik}=1/\sqrt{N} \cdot \text{EXP}(j \cdot (i-1) \cdot (k-1) \cdot a) \quad ①$$

where $k=1, 2, \dots, N$, $i=1, 2, \dots, N$ and $a=2 \cdot \pi / N$.

A matrix $[E]$ is formed using the eigenvectors of $[S]$ as columns. If the eigenvalues λ_i of $[S]$ are arranged in a diagonal matrix $[D]$, the scattering matrix $[S]$ is determined from

$$[S]=[E][D][E]^{-1} \quad ②$$

If the return losses at the input ports are measured when the input ports are excited by incident waves in proportion to each eigenvector, the scattering matrix $[S]$ can be easily calculated by using Eq.②. Figure 5 shows a block diagram to measure the return loss as eigenvalues. Eight in-phase and equal amplitude signals are extracted from an 8-way divider. The phase is changed by the length of each semi-ridged cable installed on each circulator. The resultant signals are proportional to the eigenvector and used as input signals to the combiner under test. The ratio of the test signal to the reference signal at each input port is the desired return loss.

When all the power amplifier units operate normally, the return losses of all the input ports respectively exceed 20dB. According to the locations of any failed amplifiers, the return loss at a certain input port is more than 18dB for one amplifier failure and 10 to 21dB for two amplifier failures. Variations in the return loss at a certain input port exist because different

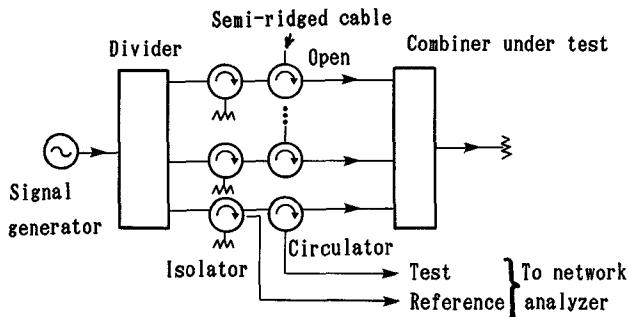


Fig.5 Block diagram to measure return loss

modes are excited corresponding to the locations of any failed amplifiers and the slits act differently on these modes.

DESIGN OF POWER DIVIDER

The power divider is a corporate type. A divider with a semicircular E-bend has been recently developed for a radial type SSPA. Using this divider, the output signals of the drive amplifier can be easily distributed to each power amplifier unit under conditions of low-loss, in-phase and equal amplitude signals. The structure of the power divider is shown in Fig.6. The divider consists of three T-junctions made of R120 waveguides. Matching of the T-junctions can be done by only one post. Also, both ends of this post are contacted to H planes of the waveguide. This is novel and quite different from conventional matching methods. The T-junction, therefore, has the merits of easy matching and high bearing power. It can be designed by deciding only the values of the diameter and the position of the matching post. These are determined experimentally. The isolation between the ports of the divider is not perfect even in theory. But this is no problem in practical use, as isolators are mounted at both the output port of the drive amplifier and the input ports of the power amplifier units.

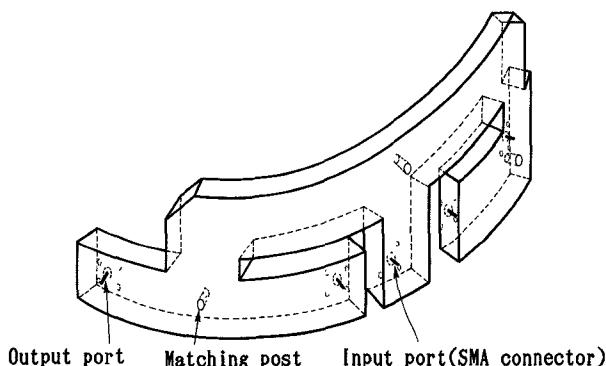


Fig.6 Structure of power divider

Figure 7 shows the characteristics of the power divider. The insertion loss is less than 0.2dB and the

return loss of the input port is greater than 20dB over the full bandwidth.

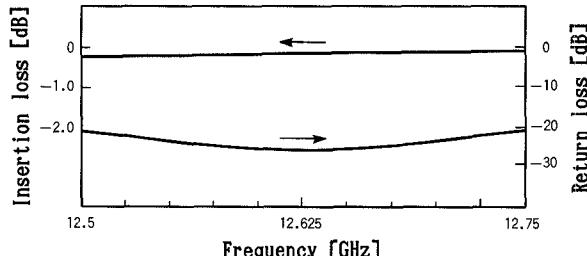


Fig.7 Characteristics of power divider

DESIGN OF POWER AMPLIFIER UNIT

The power-added efficiency of present FETs decreases with an increase in output power. The final stage of the power amplifier unit, therefore, consists of two 4W GaAs FETs with high power-added efficiency in parallel. We used a short slot type 3-dB coupler as the 2-way power combiner and a Wilkinson type 3-dB coupler as the 2-way power divider. The insertion losses of the combiner and the divider are less than 0.3dB and less than 0.9dB, respectively. The configuration of the power amplifier unit is as follows. To reduce the dimensions, the r.f. part is not connected to the 2-way power combiner on the straight, but the combiner is folded over the r.f. part. The r.f. part is put under the 2-way power combiner to have good heat flow. Typically, the output power is 39.2dBm, the efficiency including EPCs and gain are 24.1% and 17.4dB, respectively.

Each power amplifier unit and the drive amplifier have their own EPCs. The reasons are shown below. ①As the voltage supplied to each FET can be set independently, all the FETs can run under optimum conditions. The efficiency of the SSPA, therefore, can be maximized. ②As the d.c. power supply of any failed power amplifier units can be shut off, the SSPA can have graceful degradation properties. ③As the d.c. lines of the EPCs through which the large current flows can be directly connected to the power amplifier units, losses due to the d.c. current can be reduced.

PERFORMANCE OF 50W SSPA

We tested the SSPA in both air and vacuum environments. In a vacuum, namely, in the thermal vacuum test, the temperature of the baseplate of the specified power amplifier unit was controlled to equal the specified temperatures.

The principal performances of the SSPA at 23°C in air and at -10, 23, 40°C in a vacuum are shown in Table 1. In all cases, the output power at the center frequency is more than 58.8W (more than 50W over the bandwidth of 12.625 ± 0.125 GHz) and the efficiency is more than 21.6% (more than 26% excluding the EPCs). Figure 8 shows the

frequency characteristics of the output power. The differences of the characteristics between those in air and in vacuum is less than 0.2dB. This shows that the SSPA was thermally well designed. The difference of the temperature at the cases of the power amplifier units is less than 4°C. The channel temperature of the 4W FET in the final stage is estimated to be less than 90°C from the case temperature and the thermal model of the power amplifier unit. The maximum junction temperature of the transistor in EPCs is also estimated to be less than 75°C

These values are well below 110°C, which is required for long life operation.

Table 1 Principal performances of SSPA

	In Air	In Vacuum			
		23°C	-10°C	23°C	40°C
Frequency	[GHz]	12.625			
Output Power	[dBm]	48.0	48.1	48.0	47.7
Input Power	[dBm]	10.0	10.0	10.0	10.0
Efficiency	[%]	21.8	21.8	21.9	21.6
Gain Flatness	[dB _{p-p}]	0.7	0.8	0.8	0.9
Group Delay Time	[ns _{p-p}]	0.7	0.8	0.6	0.6
AM-PM Conversion Coefficient [°/dB] ^(*)		1.5	1.5	1.2	1.0

(*) maximum value

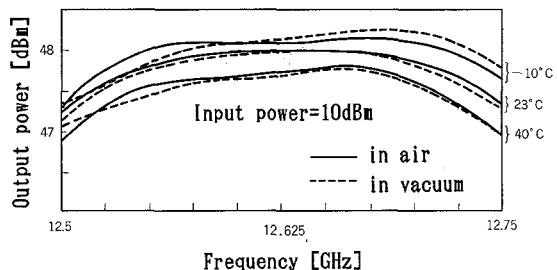


Fig.8 Frequency characteristics of output power

A thermal cycle test in a vacuum was executed. The range of the specified temperatures is -10 to 40°C. The number of cycles is 8 (about 10 hours / cycle). Two of those cycles were under conditions of no r.f. input. We could not find any problems with the SSPA during the thermal cycle test. The changes in the characteristics before and after the test were negligible.

Figure 9 shows the power degradation due to power amplifier unit failures. A abscissa presents the number of the failed power amplifier units. The reason why the number is less than or equal to 2 is that we assume the probability of failure be very small. The average values of the output power are nearly identical with a predictable $(1-M/N)^2$ graceful degradation law(3), where M is the number of the failed amplifier. This can be derived by assuming perfect isolation between the input ports of the matched combiner.

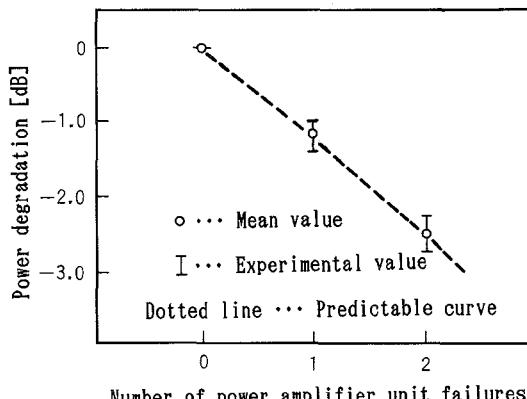


Fig.9 Power degradation of SSPA

CONCLUSION

We developed a 12.5GHz-band 50W SSPA applicable to a broad-band transponder for future broadcasting satellites. The SSPA uses an 8-way power combiner having low losses and a small size, and a pair of power dividers of semicircular E-plane bend type. A simple method calculating the S-parameters of a combiner was proposed and used to evaluate the isolation between the input ports of the 8-way power combiner. This SSPA also has graceful degradation properties. Under the thermal vacuum and thermal cycle tests, the performance of the SSPA was satisfactory, and we found that both the electrical and thermal designs are appropriate.

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